## CLAIMS

1. A voltage booster converter comprising:

- a pair of input terminals A and B for connecting a DC input voltage Vin between these two terminals;

- a pair $P_0$ of switches SB, SH in series connected by the switch SB to the input terminal B, the input terminal A being connected across an input inductor Lin to the connection point between the two switches SB and SH in series, each switch SB, SH comprising control means so as to be placed simultaneously, one in an on state the other in an isolated state;

- a pair of output terminals C and D, for powering, by an output voltage Vout, a load Rout, the output terminal D being connected to the input terminal B, characterized in that it comprises:

- K other additional pairs $P_1$, $P_2$,....$P_i$,...$P_{K-1}$, $P_K$ of switches in series with the pair $P_0$ between the output terminal C and the switch SH with i = 1, 2,...K-1, K, the two switches of one and the same additional pair $P_i$ being connected across an energy recovery inductor $Lr_i$;

- K input groups, $Gin_1$, $Gin_2$,...$Gin_i$,...$Gin_{K-1}$, $Gin_K$, of Ni capacitors C of like value each in series, with i= 1, 2,...K-1, K and Ni = i, the electrode of the capacitors of one of the two ends of each input group being connected to the common point between the two switches SB, SH of the pair $P_0$, at least the electrode of the capacitors of each of the other ends of the input groups being connected respectively to the common point between each the switch $SH_i$ and the recovery inductor $Lr_i$ of the corresponding pair $P_i$ of like rank i,

- K output groups, $Gout_1$, $Gout_2$,...$Gout_i$,...$Gout_{K-1}$, $Gout_K$, of Mi capacitors C of like value each in series, with i = 1, 2,...K and Mi=(K+1)–i, the electrode of the capacitors of one of the two ends of the output groups being connected to the output terminal C, at least the electrode of the capacitors of each of the other ends of the output groups being connected respectively to the connection point between two pairs of consecutive switches $P_{i-1}$ and $P_i$;

in that the switches of these other K additional pairs are controlled so as to form, when the switch SB of the pair $P_0$ linked to the terminal B is switched to the on state for a time Ton, a first capacitor network connected on the one hand across the switch SB to the terminal B and, on the other hand, to the terminal C, comprising the groups of input capacitors in series

with the groups of the output capacitors such that a group of input capacitors $Gin_i$ is in series with its respective group of output capacitors $Gout_i$,

and in that when the switch SB of the pair $P_0$ linked to the input terminal B is switched to the isolated state for a time Toff these other K pairs of switches form a second capacitor network connected to the terminal A across the input inductor Lin comprising the input group $Gin_K$ in parallel with the output group $Gout_1$, in parallel with groups of input capacitors in series with groups of the output capacitors such that a group of input capacitors $Gin_{i-1}$ is situated in series with a group of output capacitors $Gout_i$.

2. The voltage booster converter as claimed in claim 1, characterized in that the voltage Vout at the output of the converter is dependent on the duty ratio $\alpha$=Ton/(Ton+Toff), the capacitors C of the networks having one and the same value, the voltage Vout is given by the relation:

$$Vout = (Vin/(1-\alpha)).(K+1).$$

3. The voltage booster converter as claimed in one of claims 1 or 2, characterized in that it provides a positive output voltage Vout, the potential of the terminal A being greater than the potential of the terminal B, the potential of the output terminal C being greater than the potential of the output terminal D.

4. The voltage booster converter as claimed in one of claims 1 to 3, characterized in that the switches $SB_i$ and $SH_i$ of the additional pairs $P_i$ are diodes $DB_i$ and $DH_i$, and in that the switch SH of the pair $P_0$ connected to the pair $P_1$ is a diode DH, only the switch SB of the pair $P_0$ being retained, the cathode of a diode of a pair $P_{i-1}$ being connected to the anode of the diode of the next pair $P_i$.

5. The voltage booster converter as claimed in one of claims 1 to 4, characterized in that it comprises a first impedance $Z_i$ having a diode Ddz in series with a resistor r, the anode of the diode Ddz being linked, in the circuit of the converter, to the recovery inductor $Lr_1$.

6. The voltage booster converter as claimed in one of claims 1 to 4, characterized in that it comprises another impedance $Z_i$ having a diode Ddz in series with a Zener diode Dz, the two cathodes of the diode Ddz and the Zener diode Dz being linked together, the anode of the diode Ddz being linked, in the circuit of the converter, to the recovery inductor.

7. The voltage booster converter as claimed in one of claims 1 to 6, characterized in that each of the input $Gin_i$ or output $Gout_i$ groups respectively comprises a single capacitor $Cea_1$, $Cea_2$,....$Cea_i$.....$Cea_K$ for the input group $Gin_i$ and $Csa_1$, $Csa_2$...$Csa_i$... $Csa_K$, for the output groups $Gout_i$,

and in that the value of each of the input capacitors $Cea_i$ is deduced from the general structure by calculating the resultant capacitance of the Ni=i capacitors C in series, with i=1, 2,....K, i being the order of the input group considered:

| | |
|---|---|
| $Cea_1 = C$ | i=1 |
| $Cea_2 = C/2$ | i=2 |
| .... | |
| $Cea_i = C/i$ | i |
| ..... | |
| $Cea_K = C/K$ | i=K |

the value of each of these output capacitors $Csa_i$ being deduced from the general structure by calculating the resultant capacitance of Mi=(K+1)- i capacitors C in series, i being the order of the output group considered:

| | |
|---|---|
| $Csa_1 = C/K$ | i=1 |
| $Csa_2 = C/(K-1)$ | i=2 |
| .... | |
| $Csa_i = C/(K+1)-i$ | i |
| ..... | |
| $Csa_K = C$ | i=K |

8. The voltage booster converter as claimed in one of claims 1 to 6, characterized in that it comprises interconnections between the capacitors of one and the same level Nv of potential, the structure having a single input group Gin and a single output group Gout, and in that the input capacitor $Ceb_i$, for each of the potential levels $Nin_i$, connected between the connection points of the switches of two consecutive pairs $P_i$, $P_{i-1}$, will be deduced simply by calculating the capacitor $Ceb_i$ equivalent to the capacitors in parallel of the level $Nin_i$, of potential considered, i.e.:

$Ceb_1 = C.K$ i=1
$Ceb_2 = C.(K-1)$ i=2
....
$Ceb_i = C.((K+1)-i)$ i
.....
$Ceb_K=C$ i=K

the output capacitor $Csb_i$ of each of the levels of potential $Nout_i$, connected in parallel with its respective pair of switches $P_i$ will be deduced simply by calculating the capacitor $Csb_i$ equivalent to the capacitors in parallel of the level $Nout_i$ considered, i being the order of the output level of potential considered, i.e.:

$Csb_1 = C$ i=1
$Csb_2 =C.2$ i=2
....
$Csb_i = C.((K+1)-i)$ i
.....
$Csb_K =C.K$ i=K

9. The voltage booster converter as claimed in one of claims 1 to 8, characterized in that it comprises an output filtering capacitor Cout in parallel with the load Rout between the output terminals C and D.

10. The voltage booster converter as claimed in one of claims 1 to 2, characterized in that it provides a negative voltage, the potential of the

terminal A being less than the potential of the terminal B, the potential of the output terminal C being less than the potential of the output terminal D.

11. The voltage booster converter as claimed in one of claims 1 to 10, characterized in that the switches are semiconductors comprising a control input (control means) so as to be placed simultaneously, one in an on state through the application to its control input of a first control signal, the other in an isolated state by the application to its control input of a second control signal complementary to the first.

12. A conversion structure characterized in that it comprises several positive and/or negative converters, according to one of claims 1 to 11, in parallel.

13. The conversion structure as claimed in claim 12, characterized in that the control signals of the converters of the conversion structure are out of phase so as to reduce the input and/or output current ripples of the booster converters.